Fall 2020

ESE 118: Digital Logic Design

Instructor: Dmitri Donetski

E-mail: dmitri.donetski@stonybrook.edu

Office Hours: Tuesday, Thursday, 1-3 PM, online via Zoom.

Prerequisites: Engineering Major: ESE 123; Computer Science Major: CSE 220

Description: The course covers binary numbers, Boolean algebra, arithmetic circuits, flip-flops, analysis and design of sequential circuits, memory and programmable logic. The circuits are designed and simulated with CAD tools, assembled on breadboards and verified with the digital pattern generator and the logic analyzer.

Goal: Development of general background in theory and practical skills necessary for taking advanced courses.

Outcomes: students will develop 1) understanding fundamentals of analysis and design of digital circuits and standard building blocks; 2) skills in reading schematic of digital circuits and analysis of circuit behavior; 3) skills in design of combination and sequential circuits using conventional methods and CAD tools; 4) skills in verification and troubleshooting circuits with pattern generators and logic analyzers, determination of signal propagation delays.

Lectures: Monday, Friday, 1:00-2:20 PM, online via Zoom, see the link on Blackboard

Labs: Room 235 Heavy Eng. bldg (new addition): the lab experiments start from the 3rd week.

Section 1, Monday, 4:25-7:20 PM,

Section 3, Tuesday, 5:45-8:40 PM,

Section 4, Wednesday, 6:05-9:00 PM

Requirements: 1) Textbook: M. Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 6th or 5th edition. 6th ed: 2018, ISBN-10: 0134549899, 0134529561, ISBN-13: 9780134549897, 9780134529561, 5th ed.: 2013, ISBN-10: 0132774208, ISBN-13: 9780132774208.

2) Windows laptop or desktop for circuit design and verification (prelabs).

All homeworks, prelab assignments and instructions will be posted on Blackboard. Individual prelab reports are due by midnight before the lab session.

Grading: Lab reports (40 pts), Homeworks (10 pts), Test 1 (10 pts), Test 2 (15 pts), Final exam (25 pts).

Final grades are determined as follows: A: > 92, A-: 91-85, B+: 84-78, B: 77-71: B-: 70-64, C+: 63-57, C: 56-50 pts. Passing the course with grades in A-C range requires: 1) submission of 11 individual prelab reports (simulations) to the instructor; 2) best effort in 11 lab experiments and submission of the all final lab reports; 3) demonstration of the ability to design finite state machines on the final exam.

Topical outline:

- 1. Binary numbers and codes: 10 %
- 2. Boolean algebra, logic transformation and minimization: 10 %
- 3. Arithmetic circuits, decoders, multiplexers, latches and flip-flops: 30 %
- 4. Analysis and design of sequential circuits: 40 %
- 5. Memory and programmable logic: 10 %

Additional reading:

- F. Vahid, Digital Design with RTL Design, VHDL, and Verilog, 2nd ed, 2010, ISBN-13: 978-0470531082, ISBN-10: 0470531088
- D.M. Harris, S.L. Harris, Digital Design and Computer Architecture, 2nd ed., 2012, ISBN-13: 978-0123944245, ISBN-10: 0123944244

J. Wakerly, Digital Design: principles and practices, with Verilog, 5th ed., 2017, ISBN-13: 978-0134460093, ISBN-10: 013446009X