Spring 2019

ESE311: Analog Integrated Circuits

Instructor: Dmitri Donetski, e:mail: dmitri.donetski@stonybrook.edu
Office Hours: Tues, Thurs, 3-5 PM, 247 Light Eng.

Prerequisite: ESE372
Description: Single-stage amplifiers biased and loaded with current sources. Frequency response. Two-stage operational amplifiers designed by conventional and computer-aided techniques. Negative feedback, stability and compensation.

Lectures: 129 Physics, Mondays, Wednesdays, 2:30-3:50 PM

Textbooks: B. Razavi, Fundamentals of Microelectronics, 2nd ed., 2014, Wiley, ISBN 978-1118156322 (basic), B. Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed., 2016, McGraw Hill, ISBN-13: 978-0072524932 (adv).

Grading: 11 homeworks (11 pts), 5 simulation assignments (20 pts), project (15 pts), 2 quizzes (4 pts), test 1 (10 pts), test 2 (15 pts), final exam (25 pts)

Topical outline:

1. **MOSFET and BJT parameters**: fabrication technology of integrated circuits, - 10%

2. **Single-ended amplifiers**: biasing, active load, frequency response, Miller's theorem, cascode amplifier - 20%

3. **Differential amplifiers**: differential pairs with active load, differential gain, common-mode gain, common-mode rejection ratio, non-ideal characteristics, frequency response - 30%

4. **Negative feedback:** four basic feedback topologies, loop gain, stability and pole location, frequency compensation - 20%

5. **Operational Amplifiers**: OpAmp architectures, two-stage and folded cascode amplifiers, DC and small signal parameters, frequency response, slew rate - 20%

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Any suspected instance of academic dishonesty will be reported to the Academic Judiciary. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/uaa/academicjudiciary/

ESE311 Spring 2019: Tentative schedule

Mondays	Wednesdays	Topics
Lect. 1 1/28	Lect. 2 1/30	MOSFET and BJT characteristics. Gain of the basic cell. Comparison of the MOSFET and BJT gain stages. Current sources and sinks.
Lect. 3 2/4	Lect. 4 2/6, HW1	Current Mirrors. Biasing with voltage and current sources. Loading with current sources/sinks. Current Mirrors. Common-source (CS) stage with source degeneration. Common-Gate (CG) stages.
Lect. 5 2/11	Lect. 6 2/13, HW2	MOSFET Cascode current source. Cascode amplifier. Current steering.
Lect. 7 2/18, Quiz1	Lect. 8 2/20, HW3	Differential pairs with resistive, current source and current mirror loads. Large signal range. DC gain: differential, common mode, CMRR. 2-stage OpAmp.
Lect. 9 2/25, Quiz 2	Lect. 10 2/27, HW4	Analysis and design of CS, CG stages and cascode amplifiers. Common-drain configuration (source follower).
Test 1 **3/4**	Lec. 11 3/6	Common-emitter, common-base and common-collector stages. Improved BJT current sources
Lect. 12 3/11 Sim1	Lect. 13 3/13, HW5	MOSFET capacitances. Transition frequency. Frequency response: Poles and zeros of transfer functions. Low-pass filter, CS stage. Miller's theorem.
		Spring Break 3/18-3/24
Lect. 14 3/25	Lect. 15 3/27, HW6	Frequency response of CG stage and Cascode amplifiers
Lect. 16 4/1, Sim2	Lect. 17 4/3, HW7	Frequency response: differential gain, common-mode gain, CMRR in stages with resistive and current mirror loads
Lect. 18 4/8, Sim3	Lect. 19 4/10, HW8	2-stage CMOS OpAmp: frequency response of differential gain, frequency compensation, transient response.
Test 2 **4/15**	Lect. 20 4/17	Four basic feedback topologies
Lect. 21 4/22 Sim4	Lect. 22 4/24, HW9	Loop gain, pole location, stability, frequency compensation (review)
Lect. 23, 4/29, Sim5	Lect. 24 5/1, HW10	Regulated cascode amp. Folded cascode OpAmp: DC and small-signal analysis, frequency and transient responses, slew rate
Lect. 25 5/6, Project	Lect. 26 5/8, HW11	Review and problem solving