Spring 2017

ESE 218: Digital Systems Design

Instructor: Dmitri Donetski
E-mail: dmitri.donetski@stonybrook.edu
Office Hours: Tuesday, Thursday, 3-5PM, 247 Light Eng. bldg.

Prerequisites: Engineering Major: PHY 127 or 132 or 142, or ESE 124; Computer Science Major: CSE 220

Description: The course covers binary numbers, Boolean algebra, arithmetic circuits, flip-flops, analysis and design of sequential circuits, memory and programmable logic. The circuits are designed and simulated with CAD tools, assembled on breadboards and verified with a logic analyzer.

Goal: Development of general background in theory and practical skills necessary for taking advanced Electrical and Computer Engineering courses.

Outcomes: students will develop 1) understanding fundamentals of analysis and design of digital circuits and standard building blocks; 2) skills in reading schematic of digital circuits and analysis of circuit behavior; 3) skills in design of combination and sequential circuits using conventional methods and CAD tools; 4) skills in verification and troubleshooting circuits with a logic analyzer, determination of signal propagation delays.

Lectures: Javitz Hall 111, Tuesday, Thursday, 5:30-6:50 PM

Labs: 235 Heavy Eng. bldg.
Section 1, Monday, 8:55-11:55 AM
Section 2, Monday, 7:00-10:00 PM
Section 3, Tuesday, 7:00-10:00 PM

Textbook (required): M. Morris Mano, Michael D. Ciletti, "Digital Design", 5th ed., Prentice Hall, 2013, ISBN-13: 978-0-13-277420-8, ISBN-10: 0-13-277420-8

Lab kit (required): "ESE218" lab kit is available at the SBU bookstore, Frank Melville Library

Grading: 11 homeworks (22 pts), lab reports (22 pts), test 1 (10 pts), test 2 (15 pts), final exam (25 points), portfolio (6 points). All lab reports are required to pass the course with grade C and above.

Topical outline:
1. Binary numbers and codes: 5%
2. Logic transformation and minimization: 15%
3. Arithmetic circuits, decoders, multiplexers: 15%
4. Latches and flip-flops, registers and counters: 15%
5. Analysis and design of synchronous circuits: 30%
6. Memory and programmable logic: 20%

References:
1. M. Mano, C. Kime, Logic and computer design fundamentals, Prentice Hall, 2004, ISBN 0-13140539-X
2. A. Markovitz, Introduction to logic design, McGraw-Hill, 2010, ISBN 0-07-319164-5
3. J. Wakerly, Digital Design: principles and practices, Prentice Hall, 2006, ISBN 0-13-186389-4
4. S. Brown, Z. Vranesic, Fundamentals of Digital Logic, McGraw-Hill, 2009, ISBN 978-0-076352953-0
5. C. Roth, L. Kinney, Fundamentals of Logic Design, PSW, 2010, ISBN-13, 978-0-495-47169-1

Tentative schedule

W	Tuesdays Homeworks	Thursdays Tests	Topics	Labs
1	Lecture 1 1/24	Lecture 2 1/26	Binary numbers and codes. Binary arithmetic. Logic operations and gates.	No labs. Room 235 is closed.
2	Lecture 3 1/31 HW1	Lecture 4 2/2	Boolean algebra. Canonical and standard forms. Two-level implementations. Digital logic families. Propagation delays and glitches	Room 235 is closed. Prelab for Lab 1 (CAD software installation on PC and simulation)
3	Lecture 5 2/7 HW2	Lecture 6 2/9	Incompletely specified functions. Logic maps. Algorithmic minimization methods.	Lab 1 Board and Logic analyzer. Propagation delays
4	Lecture 7 2/14 HW3	Lecture 8 2/16	Decoders, encoders, multiplexer. Introduction to Hardware Description Languages.	Lab 2 Two-level implementations
5	Lecture 9 2/21 HW4	**TEST 1 2/23**	Review for test 1. Problem solving.	Lab 3 Decoders
6	Lecture 10 2/28	Lecture 11 3/2	Adders, subtractors, multipliers. Comparators	Lab 4 Design with multiplexers
7	Lecture 12 3/7 HW5	Lecture 13 3/9	Latches and flip-flops.	Lab 5 Adder/subtractor
			Springbreak	
8	Lecture 14 3/21 HW6	Lecture 15 3/23	Analysis and design of sequential circuits	Lab 6 State elements
9	Lecture 16 3/28 HW7	Lecture 17 3/30	Synchronous counters. Shift registers. Ring and Johnson counters.	Lab 7 Synchronizer
10	Lecture 18 4/4 HW8	Lecture 19 4/6	State assignment and reduction. Sequential multipliers and dividers. Cyclic Redundancy check.	Lab 8 Counter
11	Lecture 20 4/11 HW9	**TEST 2 4/13**	Review for test 2. Problem solving.	Lab 9 Serial data transfer 1 (scrambler/descrambler)
12	Lecture 21 4/18	Lecture 22 4/20	Asynchronous circuits, ripple counters Programmable logic devices.	Lab 10 Serial data transfer 2 (CRC)
13	Lecture 23 4/25 HW10	Lecture 24 4/27	Memory	Lab 11 Project
14	Lecture 25 5/2 HW11	Lecture 26 5/4	Review for the final exam	Lab 11 Project (cont.)
			Final exam	

If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Disability Support Services, ECC (Educational Communications Center) Building, room128, (631) 6326748. They will determine with you what accommodations, if any, are necessary and appropriate. All information and documentation is confidential.

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty are required to report any suspected instances of academic dishonesty to the Academic Judiciary. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/uaa/academicjudiciary/

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Judicial Affairs any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn.