

ESE 555: Advanced VLSI Systems Design

Fall 2023

Instructor: Dr. Emre Salman

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Office: Room 257, Light Engineering Building

Office hours: TBA

Class Meetings: Tuesdays and Thursdays 2:30 pm to 3:50 pm

Course Description:

This course describes the well established integrated circuit design process. VLSI circuit design techniques in the MOS technology are presented. Topics include MOS transistor theory, CMOS processing technology, VLSI design methodologies, MOS digital circuit analysis with emphasis on power consumption and delay/performance. Various CMOS circuit design techniques will be highlighted with emphasis on low power and high performance. Integrated digital systems are designed and simulated throughout the course using VLSI design tools. At the end of the course, students will understand and experience the conventional VLSI design flow, and gain sufficient background for more advanced courses in the field.

Course Requirements:

There will be several computer-aided design and analysis assignments throughout the course in addition to homeworks. The students are also expected to complete a design project (schematic and layout) using Cadence IC design tools.

Prerequisite:

BSc in electrical engineering/computer engineering or computer science.

Undergraduate students: ESE 330 or ESE 355.

Teaching Material:

Required

- N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition, Addison Wesley

Recommended

- E. Salman and E. G. Friedman, High Performance Integrated Circuit Design, McGraw-Hill, 2012
- E. Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, 1st edition Addison Wesley

Course Content: Course consists of the following subjects

- Introduction and motivation
- Design flow and summary of VLSI design methodologies
- CMOS fabrication flow
- Transistor theory and transistor nonidealities
- Scaling theory
- Power/energy and low power design techniques
- SPICE/Circuit analysis and simulation techniques
- Combinational circuit design and circuit families
- Sequential circuit design
- Adders and datapaths
- Memory design
- Introduction to interconnects
- Packaging, power, and clock
- CMOS reliability

Grading:

- Midterm: 25%
- CAD assignments + homeworks: 30%
- Final project: 45%

Student Learning Objectives:

- An ability to apply knowledge of mathematics, science, and engineering
- An ability to identify, formulate, and solve engineering problems
- An ability to understand current research issues

Student Accessibility Support Center Statement

If you have a physical, psychological, medical, or learning disability that may impact your course work, please contact the Student Accessibility Support Center, 128 ECC Building, (631) 632-6748, or via e-mail at: sasc@stonybrook.edu. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

Academic Integrity Statement:

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty are required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including

categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

Critical Incident Management Statement:

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Judicial Affairs any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures.